A mm-Precise 60GHz Transmitter in 40nm CMOS for Discrete-Carrier Indoor Localization

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Abstract

This paper presents a multicarrier 60GHz transmitter for distance measurement (ranging) in an indoor wireless localization system, achieving mm-precision with high update rate. The architecture comprises a baseband subcarrier generator, an upconverter, and a power amplifier. There are three key innovations, all stemming from careful hardware-algorithm co-design: 1. efficient frequency planning of the 6GHz-wide band; 2. power-efficient multicarrier signal generation by means of digital frequency divisions exploiting the phase-based time-of-arrival ranging algorithm; and 3. PAPR reduction to enable efficient operation of the power amplifier. By implementing these key techniques, 0.7-2.7mm precision is achieved over 5m measured distance with 5.4μs symbol duration. During operation, the core digital subcarrier generator generates 16 non-equidistant subcarriers from a 3GHz input clock, while consuming an average power of 1.8mW out of 0.9V supply. The upconverter and the power amplifier altogether consume around 127mW. The total area of the transmitter is 1.1mm^2. The chip is fabricated in a 40nm general purpose CMOS process.

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Index Terms

60GHz transmitter, CMOS, mm-precision, ranging, localization, positioning system, multicarrier, radar, inverse-GPS, frequency divider, time-of-arrival.

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I. Introduction

THE availability of up to 9GHz unlicensed bandwidth around the 60GHz ISM band is attractive for high precision indoor localization systems. From the technology perspective, thanks to scaling, the implementation in CMOS enables miniaturization, integration with the digital baseband, and high frequency operation up to mm-wave range.

Fundamentally, localization involves two steps, namely distance measurement (ranging) and triangulation. This work focuses on ranging since it is the precision-defining operation at the physical layer. The classification and the methods of localization have been discussed in [1]. Several applications such as sports, military, and industrial automation require high precision delivered with fast update rate. Time-of-arrival (ToA)-based UWB ranging systems are favored in such applications. Unlike angle-of-arrival and received signal strength estimations, time-based range estimation techniques improve the estimation performance by increased bandwidth and carrier frequency.

The Cramér-Rao Lower Bound [2] reveals that mm-precision with less that 1ms update rate is possible in the 60GHz band. Achievable ranging precisions of the systems operating at 2.4GHz, 5GHz, 24GHz, 60GHz, and 144GHz are theoretically calculated and compared in Fig.1. The theoretical calculations and the assumptions are given in the Appendix. The high precision ranging systems in the literature ([3]–[7]) show that the theoretical bound is credible.

As predicted by the bound, mm-wave ranging is necessary to achieve mm-precision. Several state-of-the-art mm-wave systems in CMOS such as [8] and [9] achieve sub-cm accuracy. However, in [9], the carrier frequency is 144GHz, limiting the maximum range due to high free-

space path loss. On the other hand, FMCW systems such as [8] employ time-domain multiplexing which requires ms-long ranging signal duration. Further reduction of symbol duration is achievable by frequency-domain multiplexing. Our previous work on the receiver demonstrated an additional benefit from discrete multicarrier operation, which enables subsampling, thus reducing its processing bandwidth and improving power efficiency [10].

As demonstrated in [11], an OFDM transmitter for communication can be modified for ranging, but since the OFDM bandwidth is in hundreds of MHz, only sub-meter precision can be reached. On the other hand, generating a GHz-wide multicarrier signal with an OFDM transmitter is very power hungry. This is certainly not suitable for remote localization, whereby the mobile signal emitter is expected to be a simple beacon and the energy efficency is of paramount importance.

This paper presents a solution to the challenging requirement of generating 6GHz-wide multicarrier signal efficiently at the 60GHz band, which is crucial for mm-precise ranging. By performing a co-design with the nonlinearity-tolerant algorithm, a high precision, high update rate, yet power efficient transmitter architecture is achieved. The relaxed linearity and orthogonality specifications of the ranging signal allow subcarrier generation by power-efficient digital frequency division. Thanks to this smart generation scheme, major conventional power hungry baseband blocks, such as OFDM processor and Digital-to-Analog Converter (DAC), are avoided. Moreover, symbol selection is performed to minimize the Peak-to-Average Power Ratio (PAPR) down to 3dB, which enables efficient operation of the power amplifier (PA). The proposed transmitter architecture is firstly reported in [12], whereby 0.7-2.4mm standard deviation is accomplished over 4m range. In addition to the ranging performance already reported, this paper presents the architecture and transistor-level design considerations of the signal generation. Further building blocks measurements are also presented to highlight the impact of the circuit performance on ranging. Moreover, the measured range is extended up to 5m in this work.

Section II discusses the system considerations specific to the ranging transmitter design. The

proposed discrete multicarrier transmitter architecture is presented in Section III. The implementation details are addressed in Section IV. Section V reports the measurement results in bottom-to-top fashion, starting from the characterization of the building blocks and ending with the ranging performance. The comparison with other works are also addressed in this section. Lastly, the paper is concluded in Section VI.

II. Localization System Considerations

A. Insights from the Developed Time-of-Arrival Algorithm

This work presents a hardware-algorithm co-design for an indoor wireless localization system. This system can be viewed as an inverse-GPS system, whereby the time-of-arrival (ToA) is used to determine the distance. An illustration of the localization system simplified for 2 receivers is shown in Fig.2a. Given the antenna positions as $\mathbf{P_i} = [x_i, y_i, z_i]$, the distance between a receiver position and the transmitter position, $\mathbf{P_{TX}}$, is:

$$|\mathbf{P_i} - \mathbf{P_{TX}}| = c_{Light}.\,(t_i - t_f) \tag{1}$$

where c_{Light} is the speed of light and t_i is the arrival time of the signal at the i-th receiver and t_0 is the time TX starts transmitting. Due to random delay between the instance when Master generates transmit command and TX starts transmitting, t_f is an unknown alongside x_{TX}, y_{TX} and z_{TX}. Therefore, to perform localization in 3-D with 4 unknowns, 4 base stations should be employed.

To focus on the system's ranging performance, in this paper, we will assess an equivalent 1-D localization system in which the TX and 2 RXs are aligned, as illustrated in Figure 2a. This 1TX-2RX system is capable of extracting both the TX-RX distance and the unknown firing time from the resulting problem with 2 unknowns and 2 equations. Setting Base 1 as the reference receiver, t_f is derived by

$$t_f = t_1 - \frac{r_1}{c_{Light}}. \tag{2}$$

where the distance between the transmitter and the reference receiver, r_1, is known. Hence, the distance between the transmitter and the receiver under estimation becomes

$$r = c.(t_2 - t_1) + r_1. \tag{3}$$

Therefore, the localization problem in 1-D is performed by two ToA estimations in which a precise ToA estimation algorithm in [13] is employed. The algorithm is based on the phases of discrete subcarriers which effectively fill the 6GHz bandwidth. The phase of the subcarrier i is

$$\theta_i = 2\pi f_i \tau, \tag{4}$$

where f_i is the subcarrier frequency and τ is the ToA to be estimated. The solution of (4), i.e. τ, can be graphically viewed as the slope of the phase vs frequency plot in Fig.2b.

A suitable ranging signal for this algorithm comprising N subcarriers is shown in Fig.2b and formulated as follow:

$$s(t) = \sum_{n=1}^{N} A(n).exp(2\pi i f_n t), \tag{5}$$

where f_n is the subcarrier frequency and the complex code $A(n)$ defines the initial phase and amplitude of the subcarrier. As depicted in Fig.2b, these subcarriers form an autocorrelation window (ACW). Three positive ACWs followed by three negative ACWs form the proposed ranging signal (SS). The purpose of the BPSK-like flip phase is for symbol synchronization, as the first step of the time-arrival computation algorithm. Here, an OFDM synchronization method is adapted. The widely used method [14] requires one symbol followed by the same symbol but a negative code. Intersymbol interference is avoided by consecutively transmitting the same ranging sequence and any potential interference can be avoided by tuning the highest subcarrier frequency, when necessary.

The major implication of (4) is that the ToA computation does not involve any amplitude information. Hence, amplitude linearity is not the primary concern. The algorithm allows an arbitrary selection of the number of subcarriers, their frequencies, and their code, provided that

the initial phases of the subcarriers are deterministic and the bandwidth is effectively filled. Multiple subcarrier approach provides robustness against multipath fading, which is a serious concern for indoor ranging. Therefore, by selecting the subcarriers in a smart way, the cost of signal generation on the transmitter architecture and the PAPR are reduced. The subcarriers are selected to relax the baseband signal generation, and the code is selected to minimize the PAPR. Hence, the efficiency/linearity constraints of the TX are met. The implementation of the signal generation is discussed in Section IV and the measurement results are reported in Section V.

B. Link Budget Estimation

The aim of the link budget calculation is to determine the minimum output power of the PA for a certain target Signal-to-Noise Ratio (SNR) for accurate range computation. Note that the transmitter is the DUT, whereas the receiver (RX) can be considered as a part of the measurement setup. The SNR is targeted to be 10dB at the input of the range computation. Therefore, at the receiver, it is necessary to take into account not only the thermal noise, but also the quantization noise of the ADC (P_{qnoise}). Millimeter-wave off-the-shelf components comparable to state-of-the-art CMOS implementations are used as the RF frontend [15], [16]. The ADC is implemented by oscilloscope recording whose resolution is comparable to the target receiver [17]. The quantization noise is estimated from the datasheet and the vertical setup of the oscilloscope (Agilent DPO72004B). Working backwards from the receiver to the transmitter in Table I, we can conclude that an average power of 3dBm is sufficient for 4m distance.

III. Transmitter Architecture

In communication systems, generating modulated multicarrier signals is commonly performed by OFDM architecture whereby the multicarrier baseband signal is generated by the IFFT. The signal is then converted to the analog domain by the DAC before the up-conversion to the 60GHz band. The number of bits in the OFDM processor and the DAC is allocated to meet the EVM

requirement, which is a measure of amplitude linearity to accurately represent a symbol. This is a surplus to our requirement, considering the algorithm is not using the amplitude information.

For ranging, the OFDM transmitter complexity may result in low overall transmitter efficiency because the baseband blocks and the DAC can consume energy in the same order of magnitude as the PA. Firstly, IFFT is a complex hardware operation, thus penalizing the energy consumption. This is exacerbated by the multi-Gbps wideband subcarriers generation requirement. Secondly, the DAC also operates at such high speed, drawing significant amount of power. An estimate can be drawn from [18] which is at least 30mW for 3GSps. All of these factors contribute to high power and area overhead to the whole transmitter.

An efficient generation of a 6GHz-wide discrete multicarrier signal is targeted with less than 1ms signal duration. The proposed transmitter is presented in Fig.3 whereby hardware-algorithm co-design is applied to generate a wideband multicarrier signal for favorable detection by the phase-based ranging algorithm. Such implementation stems from the prescribed signal design whose format is outlined in Fig.2b.

The transmitter is generally composed of the baseband subcarrier generator and the mm-wave frontend circuits. The subcarrier generator takes in a 3GHz input reference clock to generate n-parallel subcarriers. Subsequently, the subcarriers are simultaneously upconverted to the 60GHz band and summed, eliminating conventional analog building blocks, namely DAC. Furthermore, the signal is further amplified by a multi-stage amplifier to boost the output power. The final output has a double sideband spectrum occupying the 6GHz bandwidth.

IV. Circuit Implementations

A. Baseband Subcarrier Generator

1) Frequency Generation Architecture:

Since the target application is high precision ranging mobile transmitter, the implementation challenge is to generate a 6GHz-wide discrete multicarrier signal in power-efficient manner.

The architectural overview of the digital baseband generation scheme is depicted in Fig.4. This scheme serves two purposes: an efficient ranging signal implementation of Fig.2b and the Peak-to-Average Power Ratio (PAPR) reduction to mitigate high PAPR that typically occurs in multicarrier system, further enhancing overall efficiency.

The key essence of the proposed system level efficiency enhancement stems from the fact that the ToA computation is based on phase instead of amplitude. Hence, the amplitude linearity requirement is less stringent than OFDM, allowing the use of digital square waves and relaxed orthogonality. This permits signal generation by digital frequency division, resulting in significantly reduced complexity, compact area, and improved power efficiency.

The frequency division scheme is illustrated in Fig.4. Since the output is a double sideband spectrum occupying the 6GHz available transmission bandwidth, the highest discrete subcarrier is half of the bandwidth, thus setting the input clock to be 3GHz. The input undergoes consecutive frequency divisions by an array of differential asynchronous digital frequency dividers, whereby two groups of 7 divide-by-twos are employed, producing a total of 16 subcarriers with a format of $[SC_{16}SC_{15}...SC_1]$. The choice of 16 subcarriers is based on a compromise between ranging precision, power consumption, and PAPR. Due to the propagation delay of the divide chain, a synchronization array is added. Furthermore, as outlined in Fig.2b, the ACW control circuit flips the polarity of all subcarriers every three units of the lowest subcarrier, implemented by further dividing SC_{16} by three.

The second efficency enhancement technique by the baseband block is the PAPR reduction. One of the major drawbacks of multicarrier communication systems is that the combination of several subcarriers may result in a high PAPR as illustrated in Fig.5a. Since the average power can be significantly lower than the peak, the PA must back-off which corresponds to lower efficiency to ensure linear operation for the whole dynamic range. In the context of ranging, unlike communication systems, not all of the possible symbol permutations are required.

Therefore, several limited symbols are selected whose polarity combinations result in the lowest PAPR. Simulations are carried out in Matlab to characterize the PAPR profile of the frequency generation. The histogram is plotted in Fig.5b. Based on the profile, a fixed symbol is selected which is [11111111-111-1-111-1], reducing the PAPR from a maximum of 7dB down to 3dB.

2) Digital Building Blocks:

Differential logics are preferred to single-ended ones for implementing the digital building blocks. Despite the higher transistor count at the block level, the benefits far outweigh the hardware cost in the system level. Firstly, the nature of differential operation is best suited to implement the BPSK-like 180° ACW phase inversion, Flip Phase, in Fig.2b. Secondly, the circuit flexibility offered leads to a compact and regular layout. This is in line with the array-based architecture in Fig.4. A compact layout also minimizes parasitics enabling high frequency operation.

The frequency divider is the core of the baseband subcarrier generation. The differential static current-mode logic (CML) divider topology, depicted in Fig.6a, is typically utilized [19], [20] for high frequency dividers. The drawbacks of such circuits are mainly the DC current consumption of the tail current source and the large voltage headroom. The resistive loads are not only area consuming but also introduce high parasitic capacitance, which ultimately demand even more power for high frequency operation. In order to tackle the shortcomings of CML latches, a Differential Cascode Voltage Switched Logic (DCVSL) load [21] is applied to the latch structure, as shown in Fig.6b. The cross-coupled pMOS transistors serve both as loads and as pseudo-differential mechanism due to the positive feedback. Furthermore, by cascading two latches in master-slave configuration, depending on the presence or absence of negative feedback, a divide-by-two or a D-flipflop can be constructed, respectively, as shown in Fig.6d and Fig.6e.

The applications of DCVSL are also extended to other implemented logic blocks, namely AND/OR-gate and level shifter in Fig.6c and Fig.6i, respectively. The Dual-Edge Triggered Flipflop and the divide-by-three circuit in Fig.6f and Fig.6g, respectively, exemplify the versatility

of the DCVSL AND/OR. An array of level shifters is necessary due to the supply differences between the RF upconverter and digital blocks, which operate on 1.1V and 0.9V, respectively.

B. mm-Wave Signal Path

1) 16-Parallel Upconverters: The non-linearity tolerant ranging computation opens up the opportunity to exploit the full voltage swing of the digital generation. Thanks to this, the challenge of maintaining phase linearity can be pushed to the linear signal summation, which can be implemented by passives even at the end of the signal chain. Fig.7a depicts the proposed circuit. The upconversion is accomplished by the respective 16 identical parallel Gilbert cells. Subsequently, the upconverted signal is summed up in current-domain at the output. This particular implementation brings two benefits: measurement flexibility and linearity preservation.

The baseband signal is applied at the common-gate input whereas the 60GHz LO is applied at the common-source input. This facilitates power control without affecting the linearity of the generated subcarriers while exploiting the full swing of the digital subcarrier generation for driving the current-steering switches. Therefore, the full mm-wave signal path from LO-pin to the output can be viewed as an amplifier with current steering switches insertion. Even though beneficial for the PA operation, the PAPR reduction produces an inherent amplitude cancellation, causing a net effect of conversion loss. This problem is compensated by the high gain PA, easing the driving requirement of the LO generation due to the high gain of the overall signal chain.

The main considerations of the passive current-domain addition are linear and phase-aligned summation. Fig.8a shows the layout of the proposed current summation. The symmetric and equidistant structure is essential for good phase matching. EM simulations with ADS momentum are carried out to evaluate the mismatch. The S21 results plotted in Fig.8b demonstrate that the phase mismatches among the subcarrier paths are maximum 2.7°. Given that the 60GHz wavelength in silicon oxide is approximately 2.5mm, we can roughly estimate that this corresponds to an uncertainty margin of 0.02mm (=$2.7°/360° \times 2.5mm$) to meet the mm-precision requirement.

2) Power Amplifier: Fig.7b presents the schematic of the power amplifier (PA), which incorporates 3-stage differential transformer-coupled topology with capacitive cross-coupled neutralization for stabilization [22], [23]. The PA design essentially involves three key aspects, namely the active devices, the impedance matching network, and the stabilization method.

The active devices hold the prominent role in achieving the target output power and gain. From the link budget estimation, an OP1dB of 5dBm, thus a Psat of approximately 10dBm, is sufficient for 4m. This is achieved by biasing the output stage transistors at a current density of 0.25mA/μm and setting the width to be 128μm [24]. Furthermore, the number of PA stages is designed to provide a total of 25dB gain across the overall 60GHz signal path mainly to relax the driving requirement of the 60GHz frequency generation as illustrated in Fig.9a. Since the gain at each stage is about 14dB, to mitigate the lossy subcarriers cancellation effect, three gain stages are necessary. By working backwards, the widths of the transistors are scaled down by two to minimize the power while ensuring sufficient drive. With approximately 1-2dB/stage losses, the simulated total gain of the 3-stage PA is 38dB. On the other hand, the net conversion losses due to the parallel upconversion is 10dB, resulting in a total mm-wave path gain of about 28dB.

Transformers with overlay structure are chosen for the impedance matching network due to their excellent quality factor at high frequency [25]. They also feature numerous additional benefits, namely the compact layout and the ease of biasing provided by the center-tap. The inter-stage matching networks are optimized by complex conjugate matching. For the output stage, the matching network design is illustrated in Fig.9b. Load pull simulations are carried out to determine the optimum output impedance. Then, the output transformer is designed by maintaining a good balance between losses and hitting the target impedance, while keeping the complexity low.

Although the capacitive cross-coupled neutralization stabilizes the PA in the differential-mode,

this topology does not solve the stability problem in the common-mode. To avoid common-mode oscillations, several measures are taken, namely inserting sufficient low-Q decoupling capacitors at both gate bias and supply network [26] and providing separate supply pins for different stages. The bondwires for bias, supply, and ground are kept short to reduce the inductances.

V. Measurement Results

A. Area and Power Consumption

The ranging transmitter is implemented in a general purpose 40nm CMOS process. Fig.10a shows the die micrograph. The total area of the chip is $1mm \times 1.1mm$. The baseband subcarrier generation occupies only $125\mu m \times 100\mu m$ whereas the modulator and the power amplifier altogether occupy $500\mu m \times 1100\mu m$. Therefore, the baseband generation adds a minor area overhead to the transmitter. The remaining area is allocated for test circuits and decoupling capacitors.

The pie chart in Fig.10b provides the dissection of the measured transmitter power consumption. The chart demonstrates that the baseband block adds a minor power overhead to the transmitter in accordance to Section III despite generating a 6GHz wideband signal. During operation, the subcarrier generator dissipates a dynamic power of 1.8mW from 0.9V supply. As for the mm-wave blocks, the upconverter draws 25mA from 1.1V supply and the power amplifier consumes 110mA from 0.9V supply.

B. Subcarrier Generation Performance

The timing imperfections in the baseband signal generator set the baseline of the achievable precision. Reference clock phase noise and the frequency division process influence jitter on the generated square waves. The setup in Fig.11a is configured to evaluate the jitter at the output of the transmitter. In this setup, 20 bursts of 0.3μs duration are downconverted and recorded, right at the output of the transmitter. The phases of the subcarriers are plotted in Fig.13b.

The effect of the phase noise on the TOA estimation performance is alleviated by the linear regression (LMS linearization) step of the TOA algorithm. With this setup, for 0.3μs bursts, a standard deviation of 0.67mm is obtained as shown in Fig.11b.

C. mm-Wave Signal Path

The test flexibility of the transmitter architecture facilitates the characterization of the mm-wave path without fabricating additional stand-alone blocks. In this manner, the blocks can be characterized closer to the actual matching network condition. The signal chain from the LO-port to the output-port can be viewed as an amplifier by setting the subcarriers with a fixed code equivalent to the average power. The following mm-wave characterizations are performed with GSG probes (Picoprobe Model 67a).

Fig.12 shows the measurement setup and the results of the S-parameters. The high S21 value (28.5dB) relaxes the driving requirement of the 60GHz frequency generation block. The measured 3dB bandwidth is 7GHz, which is adequate for the bandwidth requirement. The S11 and S22 are lower than -10dB for at least 8GHz around the ranging frequency. The Edwards-Sinsky μ-factor is preferred [23], [27] since the resulting stability number quantifies the stability better, the higher is the number, the more stable is the DUT. The amplifier is unconditionally stable since $\mu > 1$ and $\mu' > 1$.

The setup in Fig.12a can also be utilized to measure AM-PM distortion using the power sweep setting of S21. The significance of this measurement is that since the phase linearity is critical for the ToA computation, AM-PM distortion should be avoided. The results in Fig.12d demonstrate that the maximum output power for an AM-PM distortion of less than 1° is about 6dBm. This enables the PA to operate at an average output power of 3dBm, thus meeting the link budget requirement. The linearity of the measured estimated vs real distance in Fig.16a suggests that the AM/PM distortion effect at this output power level is minimal.

The large signal measurements are performed using the setup in Fig.13a. The measurement

results in Fig.13b show that the output P1dB is greater than 5dBm over the ranging frequencies. Furthermore, the measured peak drain efficiency is shown in Fig.13c. The minor total drain efficiency reduction from that of PA, is consistent with the transmitter architecture's goal i.e. power overhead reduction.

D. Ranging Performance

The output spectrum of the transmitter is shown in Fig.15, demonstrating the frequency division scheme conceptualized in Fig.4. Since the detection algorithm is based on phase information, the harmonic-rich spectrum due to the square waves does not affect the detection.

A 1-D indoor wireless localization system is built to evaluate the effectiveness of the proposed transmitter as ranging signal generator, as illustrated in Fig.14a. The precise ranging technique discussed in Section II is applied. A pair of horn antennas are used. Using a ruler guide rail, the distance between TX and RX2 is measured from 40cm up to 500cm with 46 distance points. The mm-wave interface to and from the chip is carried out by probing. An AWG generates the 3GHz input clock. Since the minimum IF frequency of the mixers is 1GHz, the upconversion is performed with 57GHz LO, whereas the down conversion is done with 62GHz LO. Hence, an IF signal from 2GHz up to 8GHz is generated. The output of the downconversion is then captured by the DPO Tektronix oscilloscope with 50GS/s sampling rate.

Fig.14b shows the timing diagram of the measurement. Besides providing the clock, the AWG is also programmed to control the RESET sequences and the ranging bursts. At the falling edge of RESET signal, the chip starts transmitting at t_f and, at the same token, the oscilloscope recording is triggered. A ranging burst consisting of 7 synchronization sequences (SS) with a total length of $5.4\mu s$ is transmitted, which defines our symbol duration. Note that the aim of collecting 100 samples is to provide good statistical profile of distances, i.e. standard deviation and mean. The ranging algorithm is then run in Matlab on each set and the results are plotted in Fig. 16a. From the entire dataset (100 samples$\times$46 distance points), only 22 outliers causing

measurement errors larger than 80cm are detected and discarded. The precision, defined as the standard deviation of the measured error, is between 0.7-2.7mm.

The linearity and the monotonicity of the plot confirm that the harmonic-rich spectrum in Fig.15 does not affect the accuracy since the ToA computation depends only on phase. This allows the implementation using simple digital dividers with higher energy efficiency than the conventional OFDM transmitter. Moreover, since the AM/PM distortion is negligible at 3dBm, excellent ranging linearity and precision are achieved. Fig.16c further demonstrates that the measured precision degrades as the PA reaches saturation.

The estimation algorithm is also robust against clock offset. Fig.16b demonstrates that there is no significant difference in ranging accuracy whether or not the transmitter shares a common reference clock with the receivers. Therefore, the proposed system is suitable for mobile applications where the TX and RX clocks are separated.

In the context of ranging signal generation, Table II compares this work with the state-of-art mm-wave high precision distance measurement transmitters in silicon. Despite the focus on the transmitter, the evaluation of the signal generation's ranging capability also involves receivers with components comparable to the state-of-art CMOS. This work demonstrates the best measured precision, consistent mm-precision over 4m range, while offering competitive performance at other aspects. In a broader context, UWB CMOS implementation can also achieve mm precision [7], [28]. However, since the signal generation is not addressed in this receiver-centric system, a fair comparison on the transmitter is not feasible.

VI. Conclusion

A discrete-multicarrier 60GHz transmitter architecture for localization is proposed. A careful hardware-algorithm co-design results in an energy-efficient ranging signal generation which effectively fills the 6GHz-wide available bandwidth, while simultaneously achieves excellent precision. Since the range computation solely depends on phase information, we demonstrate that

the measured distance is linearly proportional to the real distance in spite of the amplitude non-linearity and not being strictly orthogonal. These factors enable power efficient signal generation by digital frequency division, eliminating power hungry building blocks such as OFDM processor and DAC. The measurement results demonstrate 0.7-2.7mm standard deviation, measured until 5m. The short symbol duration of 5.4μs ensures efficient energy consumption. The symbol selection reduces the PAPR to 3dB which enables efficient operation of the power amplifier.

ACKNOWLEDGMENT

This project is funded by Flemish Agency for Innovation by Science and Technology (IWT) as SBO project OmniTrack. The authors would like to thank F. Daenen, N. Gaethofs, T. Redant, N. Deferm, and TELEMIC for measurement support and discussions.

APPENDIX

The Cramer-Rao Lower Bound for ToA estimation is derived in [2] as

$$\sigma^2 \geq \frac{3}{4\pi^2\, T\, \mathrm{SNR}\Big((f_c+\frac{B}{2})^3-(f_c-\frac{B}{2})^3\Big)} \tag{6}$$

where B is the bandwidth of the signal, f_c is the center frequency, T is the signal duration and SNR is the signal to noise ratio. There are 5 bands being compared in Fig.1. The bandwidth of these bands and maximum allowed transmission power is limited by FCC (Federal Communications Commission) as given in Table III.

SNR at the receiver is calculated as,

$$SNR = P_{TX} - N_{kT} - P_L - NF \tag{7}$$

where P_{TX} is transmitted power, NF is noise figure of the receiver, P_L is free space loss and N_{kT} is thermal noise. Thermal noise is calculated as

$$N_{kT} = -174 + 10log(B). \tag{8}$$

Free space loss P_L at $d = 10$ m is,

$$P_L = 10log\left(\frac{2\pi d}{\lambda}\right)^n \tag{9}$$

where λ is wavelength of the center frequency and n is 1.55, for Line-of-Sight channel.

Using these equations and the values in Table III, received SNR at 10 m distance is calculated. Then,the SNR is fed into the Cramer Rao bound in (6), where signal duration T = 1 ns for all bands.

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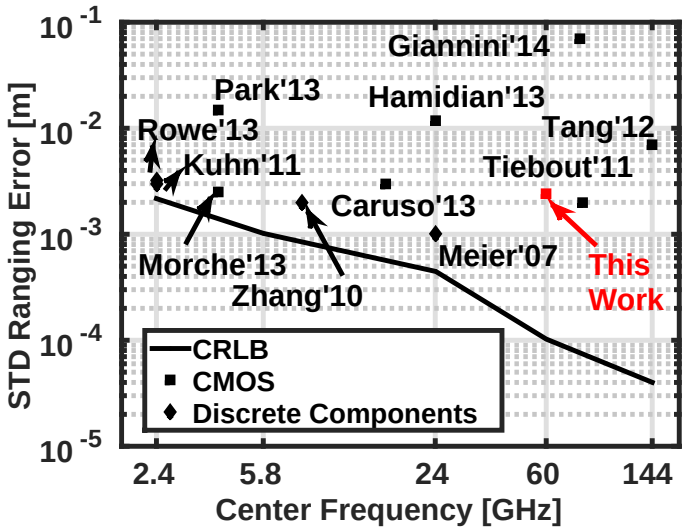
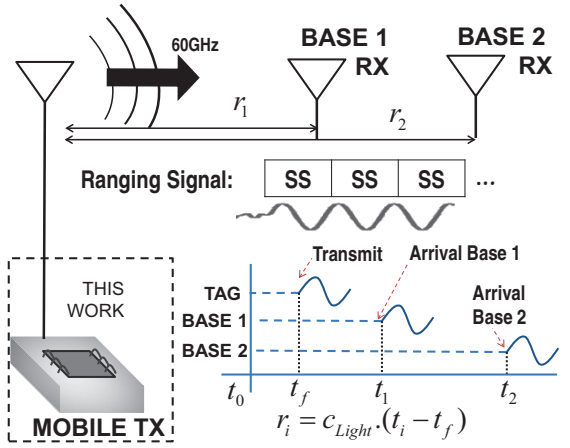
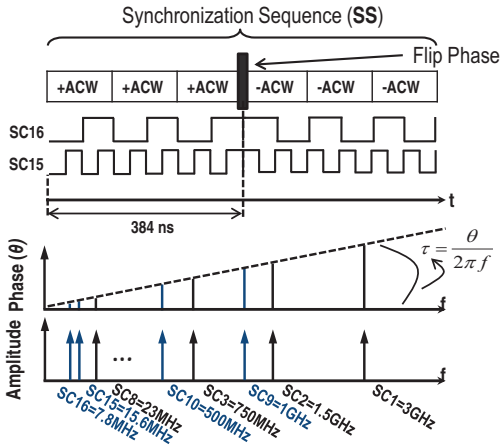


Fig. 1. High precision distance measurement system state-of-the-art.



(a) 1-D Time-of-Arrival (ToA)-based localization system. Two hardware entities: the mobile transmitter as signal emitter and the fixed base receivers as the ToA measuring unit.



(b) The proposed ranging signal format. Each Synchronization Sequence (SS) is made of a pair of 3 ACWs, which is further composed of 16 subcarriers. For simplicity, only the fundamentals are plotted. The ToA (τ) is the solution of (4), i.e. graphically the slope of the phase vs subcarrier response.

Fig. 2. 1-D Time-of-Arrival (ToA)-based localization system and ranging signal format

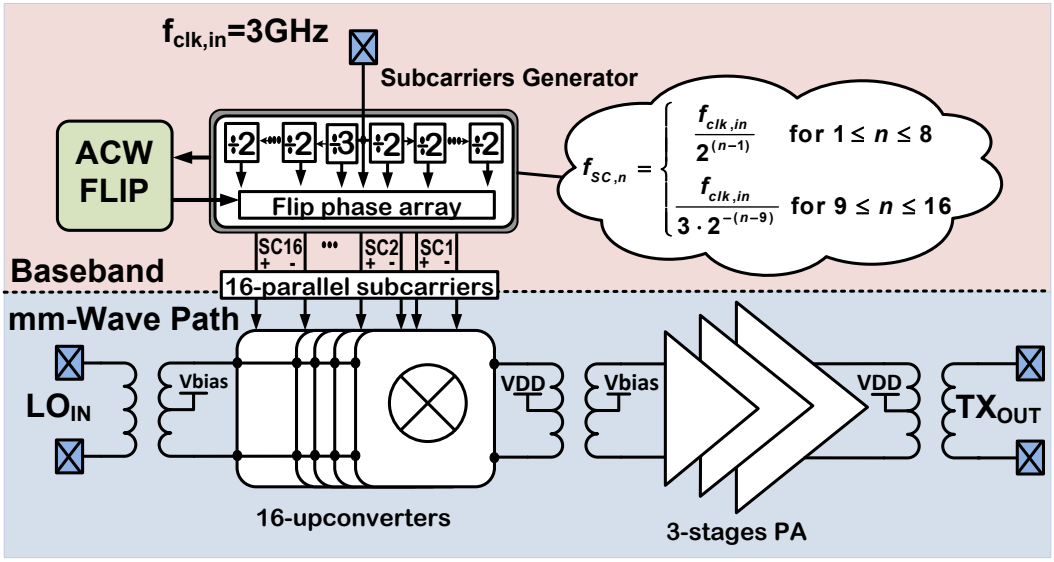


Fig. 3. The proposed 60GHz ranging transmitter architecture.

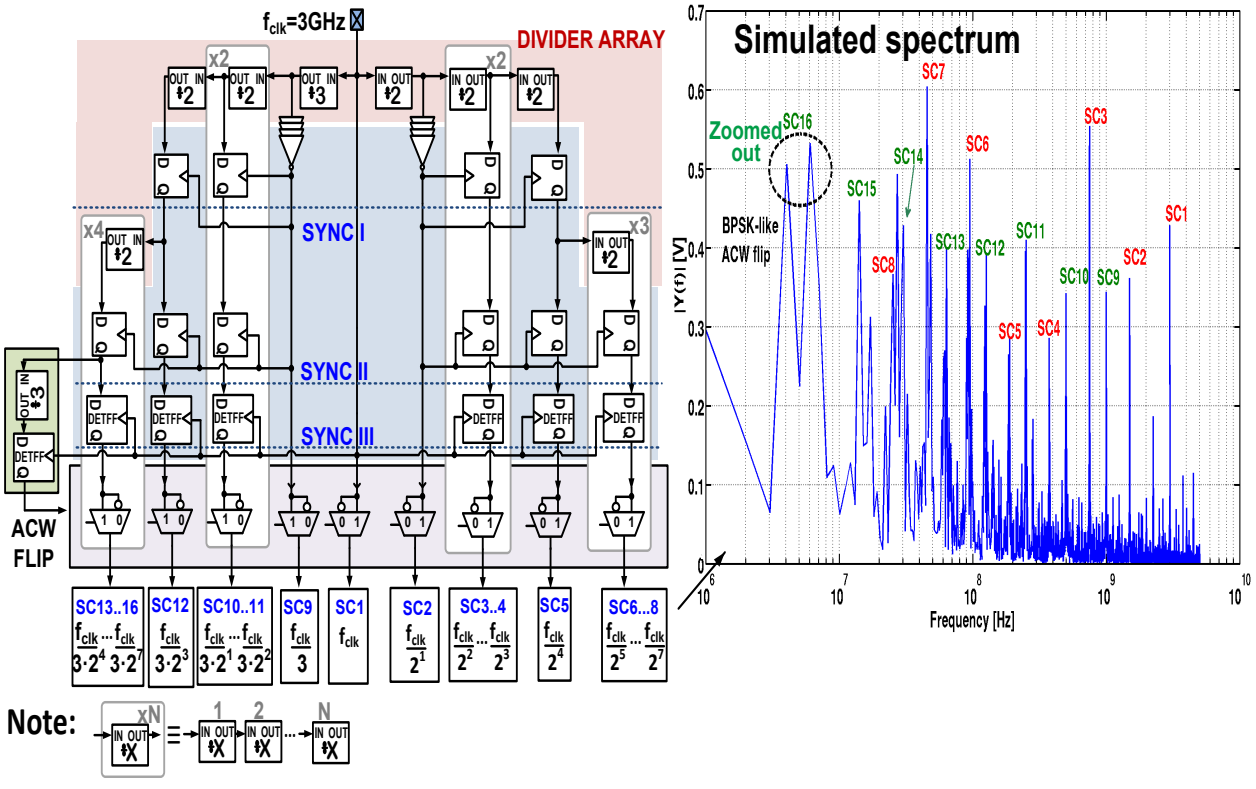
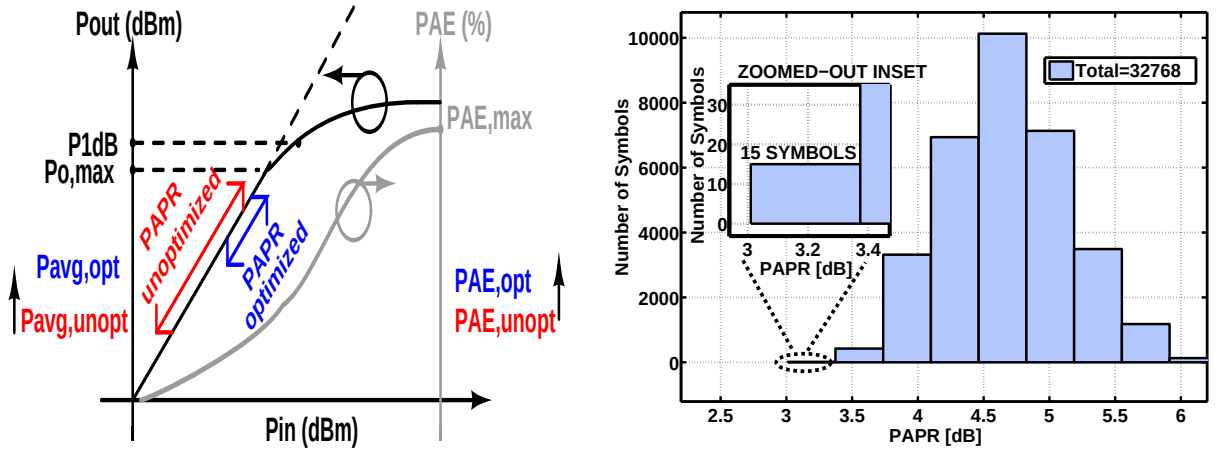


Fig. 4. Subcarrier generation by frequency division array to implement Fig.2b. Note that the figure is drawn single-ended instead of differential for simplicity.



(a) Illustration of the effect of the PAPR to the power amplifier (PA) operation.

(b) Simulated PAPR histogram of all of the symbol combinations of the proposed signal design and the ranging symbol selection.

Fig. 5. Peak-to-Average Power Reduction (PAPR) by symbol selection. The selected symbol is 11111111-111-1-111-1.

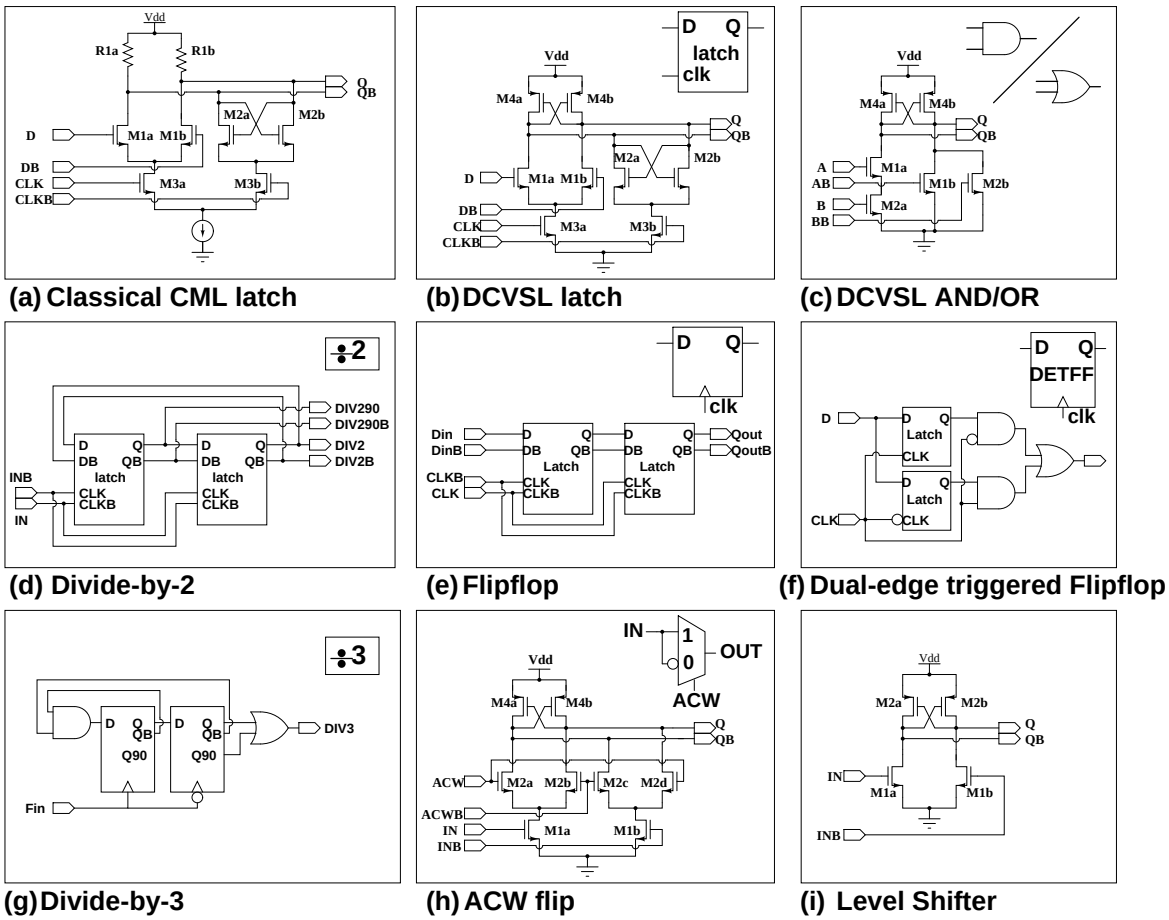


Fig. 6. Digital building blocks of the baseband subcarrier generation.

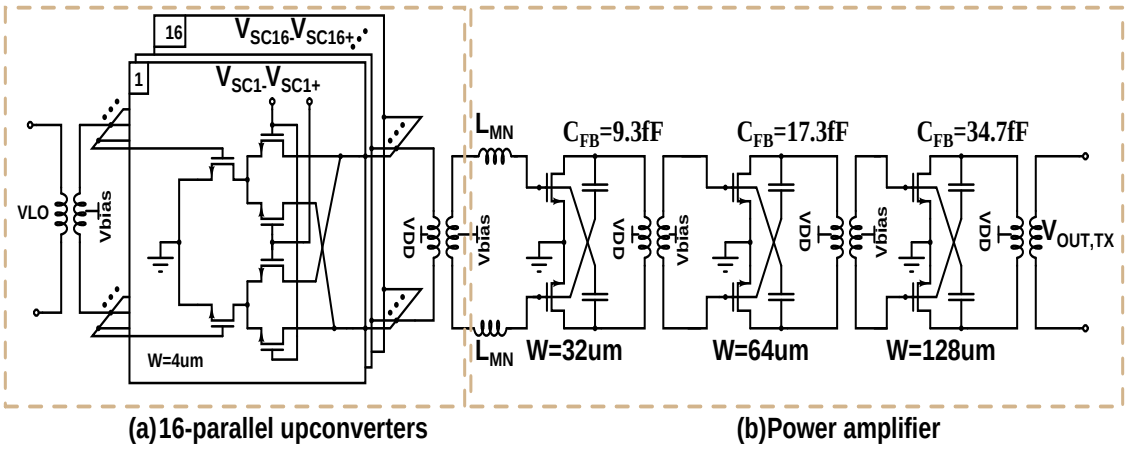
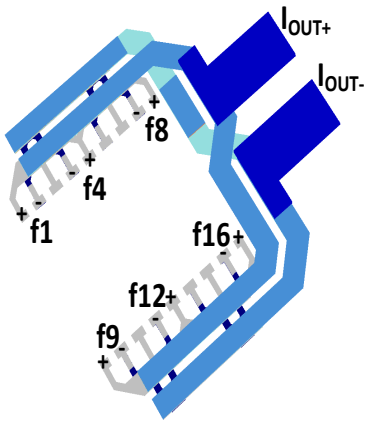
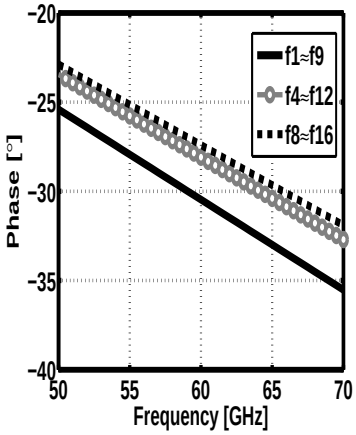


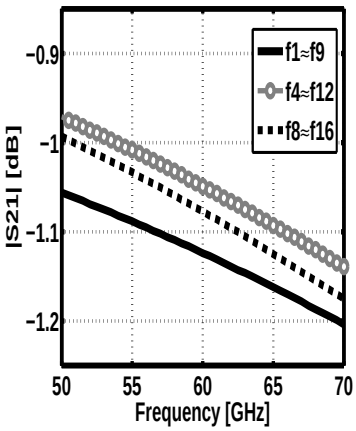
Fig. 7. Millimeter-wave signal path consisting of 16 parallel upconverters and a 3-stage transformer-coupled power amplifier.



(a) Current addition layout.

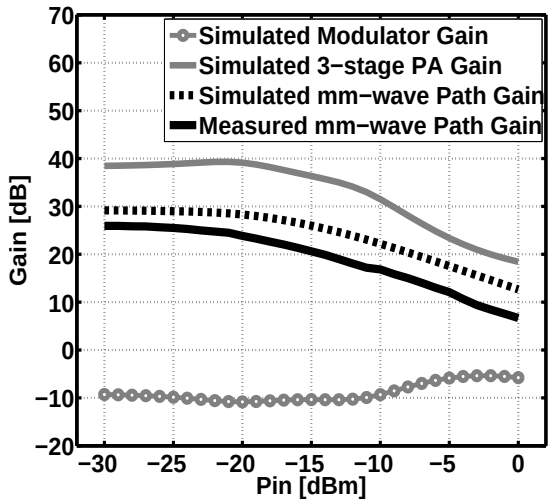


(b) Simulated phase difference of subcarrier paths.

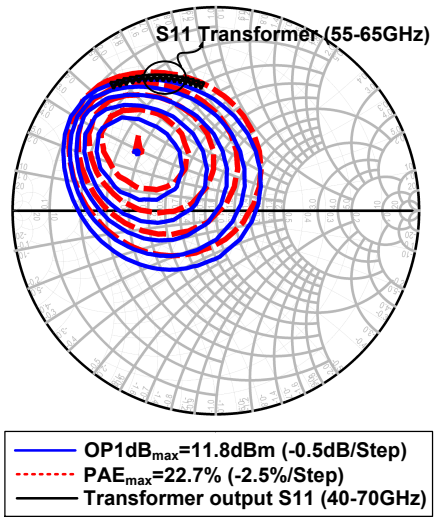


(c) Simulated magnitude difference of subcarrier paths.

Fig. 8. Current addition at the output of the parallel upconverters.

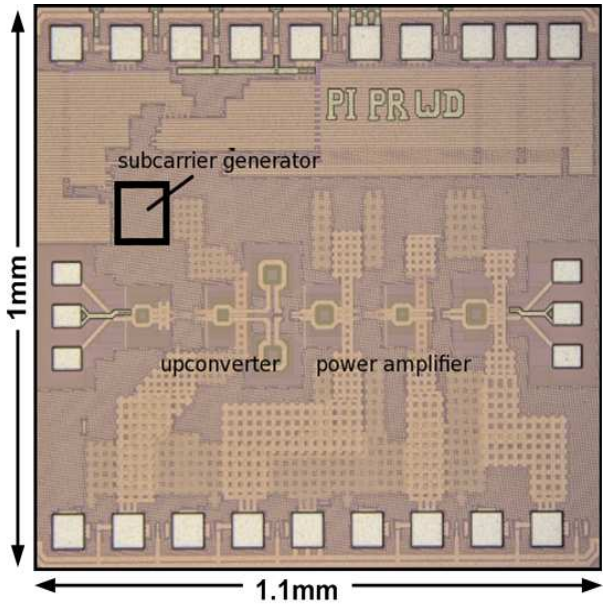


(a) Millimeter-wave signal path simulated gain breakdown.

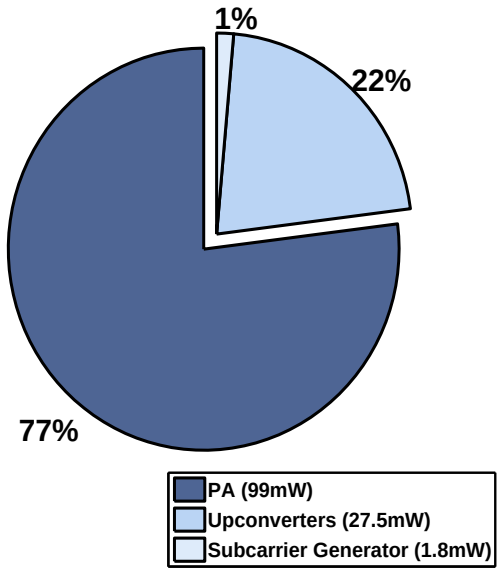


(b) PA output stage impedance matching by presenting the output transformer's input impedance to the simulated load pull power contours.

Fig. 9. Power amplifier design: gain breakdown profile and load pull simulation.

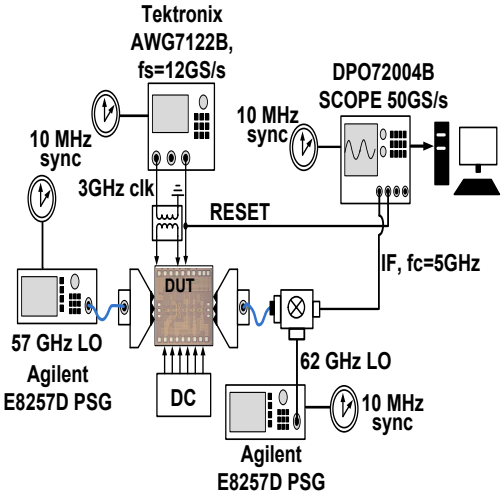


(a) Chip micrograph: The active area is dominated by the 60GHz blocks wherein the subcarrier generator occupies only $125\mu m \times 100\mu m$.

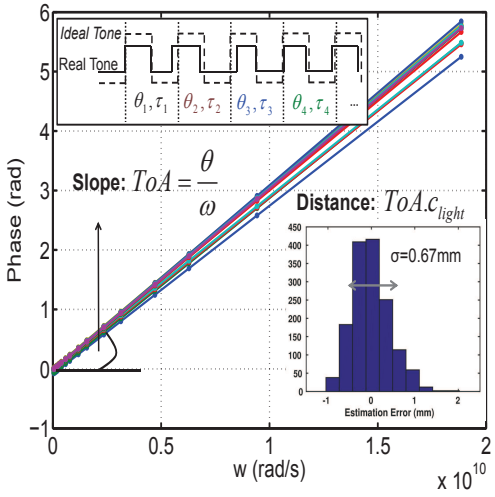


(b) The measured transmitter power consumption breakdown.

Fig. 10. Area and power consumption of the proposed transmitter.

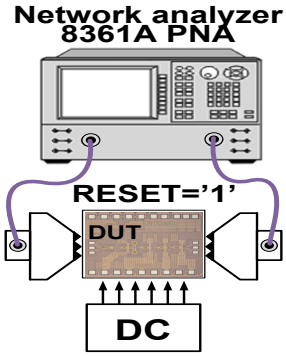


(a) Transmitter jitter measurement setup.

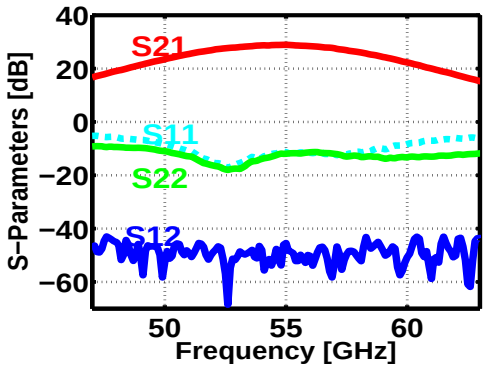


(b) Transmitter jitter measurement results.

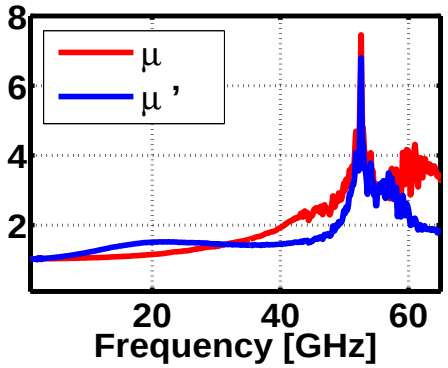
Fig. 11. Setup and measurement results of the transmitter's inherent time-of-arrival deviation due to jitter in the subcarrier generation.



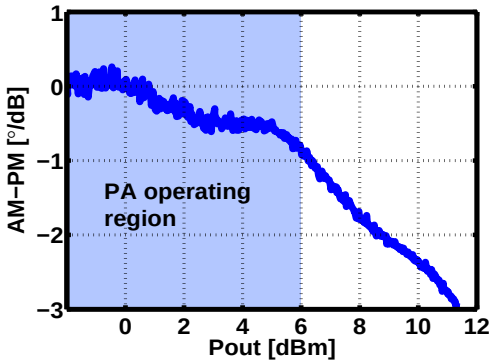
(a) The mm-wave path S-parameter measurement setup. The subcarrier inputs are internally set to a fixed static code with RESET='1'.



(b) The measured S-parameters of the mm-wave path.

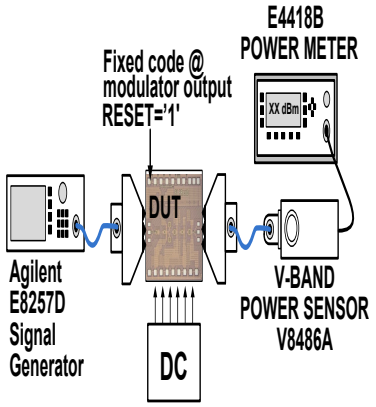


(c) Measured stability of the S-parameters.

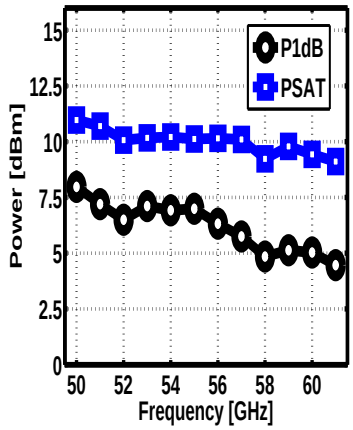


(d) AM/PM measurement results at 57GHz.

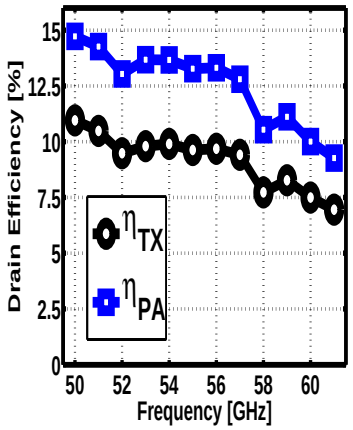
Fig. 12. S-parameter setup and measurement results of the mm-wave path (LO-TX output.)



(a) The mm-wave signal path large signal measurement setup. The RESET signal forces the subcarrier inputs to a static code.

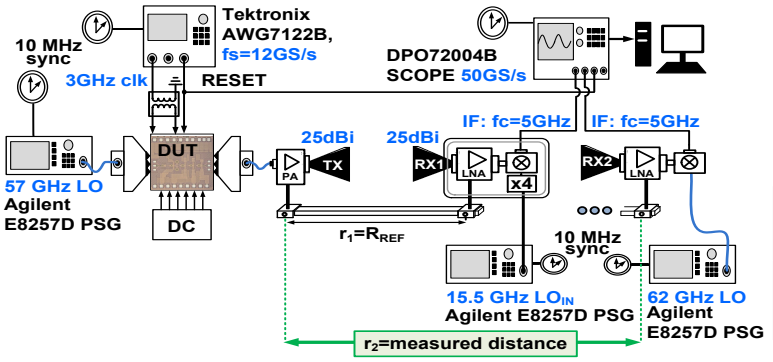


(b) Measured Psat and Output P1dB of the mm-wave path.



(c) Measured peak drain efficiency of the transmitter and the power amplifier.

Fig. 13. Large signal measurement setup and results of the mm-wave path (LO-TX output).



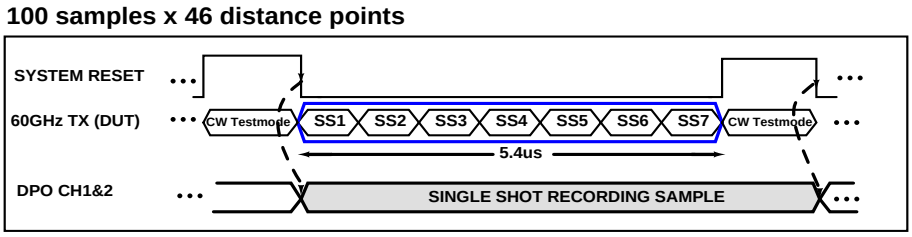
DPO72004B settings

Parameters	Value
ENOB	5.4bits
Sample Rate	50GS/s
Bandwidth	15GHz
Record Length	200k

RX settings

RX	Device	NF (dB)	Conv. Gain (dB)	Input P1dB (dBm)
RX1	Siversima FC1003V/01	8	10	NA
RX2	- V band LNA: RPG - Mixer: Millitech 15-rfsl	5	>25	<-30

(a) 1D localization range measurement setup.



(b) Ranging measurement timing diagram.

Fig. 14. Ranging setup and measurement timing diagram.

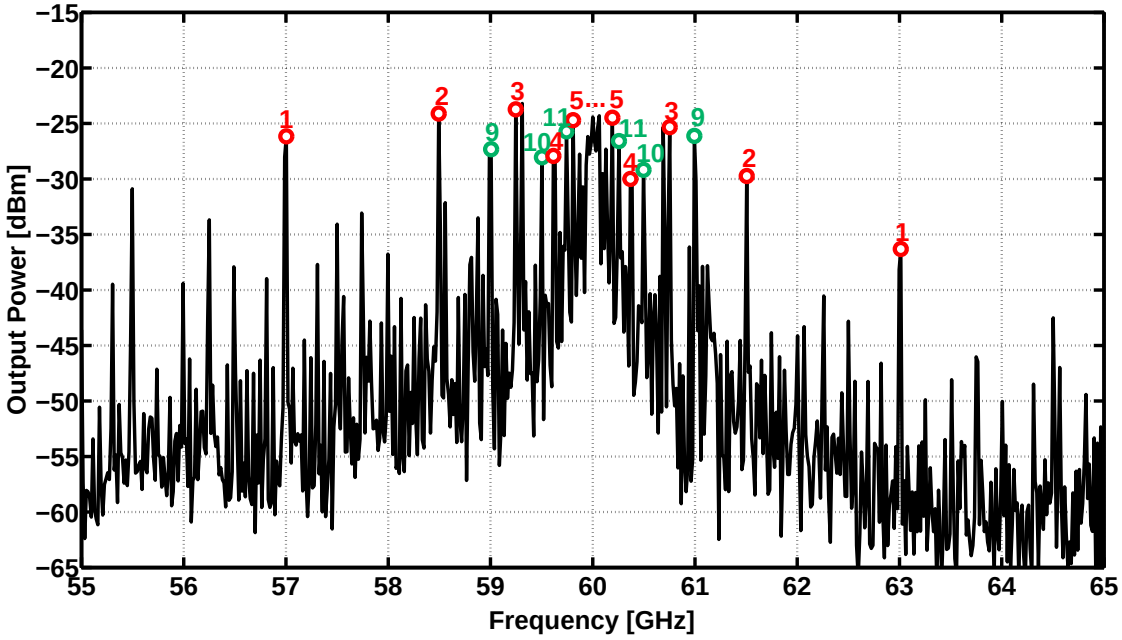
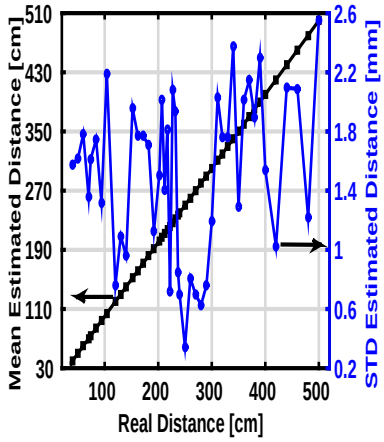
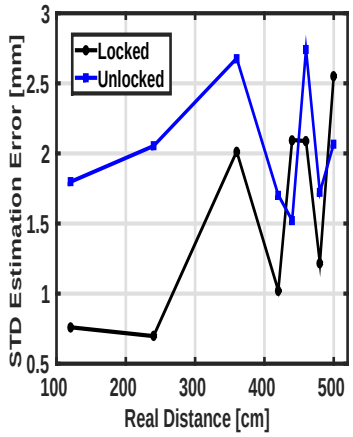


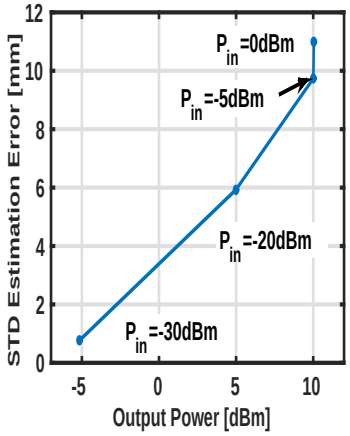
Fig. 15. The measured transmitter double-sideband output spectrum demonstrating the non-uniform tone spacing due to the frequency division scheme in Fig.4. The subcarrier indices and the respective baseband frequencies are defined in Fig.4. With f_{LO}=60GHz and f_{clk}=3GHz, the subcarriers span from 57GHz to 63GHz. Note the frequency linear scale here in contrast to the log scale in Fig 4.



(a) Ranging measurement results with common reference demonstrating mm-precise, linear, and monotonic range profile.



(b) Measured common (locked) vs separated (unlocked) reference clock between TX and RX.



(c) Measured precision degradation due to PA nonlinearity.

Fig. 16. Ranging measurement results.

TABLE I
LINK BUDGET ESTIMATION

Parameter	Gain/Loss [dB]	Power Balance [dBm]
$SNR_{DPO,out} = 10dB$		
Total noise power at the DPO output 1.DPO ADC quantization noise -ENOB=5.4 bits -Vertical setting=20mV/div -$LSB = \frac{10V_{div}}{2^{ENOB}}$ $P_{qnoise} = 10log(\frac{LSB^2}{12}) + 30$ [dBm] 2. RX Frontend -$G_{LNA+MIXER} \approx 20dB$ -NF$\approx NF_{LNA}$ =5dB -B=6GHz At the the RX frontend input $P_{noise,ch} = 10log(kTB) + 30$ [dBm] At the RX frontend output/DPO input $P_{noise,ch@DPO_{in}} = P_{noise,ch} + G_{LNA+MIXER} + NF$ Since $P_{qnoise} \gg P_{noise,ch@DPO_{in}}$ $\rightarrow P_{noise,total} \approx P_{qnoise} = -27dBm$		-27
$P_{out,DPO} = SNR_{DPO,out} + P_{qnoise}$		-17
$G_{LNA+MIXER}$	20	
RF Frontend input power $P_{RX,in}$		-37
Channel effect -d=4m -Carrier frequency=60GHz From the Friis equation, the Free Space Path loss (FPL) $FPL = 20logd + 20logf + 20log(\frac{4\pi}{c}) = 80dB$ $G_{TX,antenna} = 20dBi$ $G_{RX,antenna} = 20dBi$ $G_{channel,total} = G_{TX,antenna} + G_{RX,antenna} - FPL$	-40	
Average transmitted output power $P_{TX,out}$		3

TABLE II
COMPARISON OF HIGH PRECISION RF/MM-WAVE TRANSMITTER IMPLEMENTED IN SILICON

Specification	This work	[29] [8]	[9]	[30] [31]	[32]	[33]	[34]	[35]
Architecture	Discrete multicarrier	FMCW	Phased Radar	CW Radar	Phased Radar	Pulse Radar	Stepped Freq. Radar	PMCW Radar
Bandwidth	6GHz	250MHz	400MHz	40MHz	400MHz	10MHz/2GHz	N.A.	4GHz
Frequency	60GHz	24GHz	144GHz	72-84GHz	155GHz	3-5GHz	2-16GHz	79GHz
Symbol duration (integration time)	5.4μs	1ms	2μs	N.A.	N.A	100μs	N.A.	$\approx$10ms Dwell Time
Precision (Worst case)	2.7mm	11.8mm	7.6mm	2mm	5.8mm	15mm	3mm (body) 9mm (air)	7.5cm
Distance	5m	2m @precision measurement	1m	50cm	60cm	10m	N.A.	2.4m @precision measurement
TX power consumption	129mW	26mW	219mW	181mW /channel	90mW	0.5mW @10MHz	N.A.	121mW
TX total area	1.1mm^2	2mm^2 (TRX)	1.82mm^2	4.44mm^2 (TRX)	1.08mm^2	3.27mm^2 (TRX)	1.3mm^2 (TRX)	1.32mm^2
Pout	10dBm Psat	5dBm Psat	10.1dBm Psat	$>$0dBm Psat	9.1 Psat	-3dBm Pavg	-14dBm Pavg	11dBm
Technology	40nm CMOS	130nm CMOS	65nm CMOS	SiGe:C Bipolar	65nm CMOS	130nm CMOS	65nm CMOS	28nm CMOS
LO generation	off-chip	off-chip	on-chip	off-chip	on-chip	off-chip	on-chip	1/2 off-chip
TX antenna Gain	25dBi	14dBi	-10dBi	N.A.	-9dBi	N.A.	N.A.*	25dBi(std horn) 0dBi (target)
Estimated EIRP	28dBm	19dBm	0dBm	N.A.	-1.2dBm	N.A.	N.A.	36dBm (horn) 11dBm (target)

*Antenna-skin-antenna loss is maximum 20dB; Antenna-tumor-antenna loss is maximum 160dB

TABLE III
BAND PROPERTIES

Center Freq. (GHz)	Bandwidth (GHz)	Max. allowed transmission (dBm)
2.4	0.08	52
5.8	0.15	53
24.125	0.25	50
60	6	52
144	30	52